REMARKS

Applicant thanks the Examiner for recognizing that claims 14, 20, 32 and 34 contain allowable subject matter.

Claims 1-35 are pending for further examination.

Claim 35 has been added and recites a method which corresponds to allowable apparatus claim 14. Accordingly, applicant requests entry of dependent claim 35.

Examiner Interview

Applicant thanks the Examiner for participating in a telephone interview with the applicant's representative on February 2, 2007 in which the applicant's representative explained that the Starr et al. patent did not disclose or suggest "causing to commence processing of [a] first enqueue or dequeue request prior to completion of processing [a] second enqueue or dequeueu request" as recited in present claim 1. No agreement was reached.

Claim Rejections

Claim 1 was rejected as unpatentable over Starr et al. (previously discussed) in view of Westbrook et al. (U.S. Patent No. 7,092,393). In particular, the final Office action alleges (pgs. 2-3) that an SRAM controller 214 in the Starr et al. patent commences "processing of [a] second [enqueue or dequeue] request prior to completion of processing [a] first [enqueue or dequeue] request" as recited in present claim 1. Applicant respectfully disagrees and, in view of the following remarks, requests reconsideration and withdrawal of the claim rejection.

The Starr et al. patent discloses a queue manager 220 which helps manage a queue array 200 formed of both SRAM 206 and DRAM 203 data storage units (*see* FIG. 1; col. 4, lines 20-22, 30). The queue manager 220 is responsible for managing the movement of queue entries between the queues and a microprocessor 208, transmit sequencer 215 and receive sequencer 212 (*see* FIG. 3; col. 4, lines 58-62). Requests to transfer data to and from the queues are sent to the queue manager 220 and are handled by Arbiter 235 (*see* FIG. 5). Arbiter 235 determines which of the received requests will be used by the queue manager 220 in a next cycle (col. 5, lines 2-4).

To enable high frequency operation, the queue manager 220 is pipelined, with registers 238, 240 providing temporary storage (col. 5, lines 4-9). The actual read and write requests are serviced by SRAM controller 214 by reading the tail or writing the head of an accessed queue (col. 5, lines 36-40).

The Office action asserts that since the queue manager 220 is pipelined, the servicing of the read and write requests by SRAM controller 214 corresponds to the claimed "processing of [a] second [enqueue or dequeue] request prior to completion of processing of [a] first [enqueue or dequeue] request." Applicant respectfully disagrees. The pipelining of queue manager 220 merely allows the incoming requests to be temporarily stored in registers 238 and 240 (col. 5, lines 4-9). Accordingly, the pipelining of queue manager 220 is in reference to the storage of the requests and not the processing of the requests, as recited in present claim 1. The Starr et al. patent does not disclose or suggest that the requests are processed during storage in registers 238, 240. Indeed, the *processing* of a request is more analogous to what the Starr et al. patent refers to as the "servicing" of read and write requests performed by SRAM controller 214.

Furthermore, the Starr et al. patent appears to teach the opposite of what is recited in claim 1, *i.e.*, that second enqueue or dequeue requests are processed *after* the completion of processing a first enqueue or dequeue request. For example, the Starr et al. patent discloses that status registers (265, 270, 275 and 280, *see* FIG. 5) within the queue manager 220 signal to the Arbiter 235 that a previously requested operation *was fulfilled* to inhibit duplication of requests (col. 5, lines 26-29). Accordingly, by signaling that an operation is fulfilled to prevent duplication of requests, the Starr et al. patent indicates that processing of a second request does not begin until *after* processing of a first request has been completed.

The Westbrook et al. patent discloses methods for distributed reassembly of data packets but does not disclose or suggest causing to commence "processing of [a] second [enqueue or dequeue] request prior to completion of processing of [a] first [enqueue or dequeue] request" as recited in present claim 1.

The Office action also alleges (pg. 3) that it would have been obvious to combine the features of the Westbrook et al. patent with the Starr et al. patent to "implement a cached

memory distribution as disclosed by Westbrook in the enqueue-dequeue operation as disclosed by Starr." Applicant respectfully disagrees.

The Westbrook et al. patent discloses a method of reassembling data packets that happen to arrive out of order at a particular destination, by means of packet redistribution and resequencing (col. 1, lines 36-43; col. 2, lines 48-50). To accomplish this task of reassembly, the Westbrook et al. patent discloses an architecture which includes distributed resequencing and reassembly components 303A-D (*see* FIG. 3; col. 11, lines 1-6). Received packets are distributed by a packet plane switch 301 to the four distributed resequencing and reassembly components 303A-D. The packets then are passed to a packet resequencer 402 within each of the components 303A-D (*see* FIG. 4A). Each resequencer 402 includes a local data structure 440 that identifies packet headers received and stored locally in that particular component (*e.g.,* component 303B). Each resequencer 402 also includes a global data structure to identify packet headers which are stored in other components (*e.g.,* components 303A, C-D) (col. 11, lines 64-65; col. 12, lines 16-18). The local and global data structures are updated and stored in data structure cache RAM 514 of each resequencer 402 (*see* FIG. 5; col. 12, lines 64-66).

Although the Westbrook et al. patent discloses that the data structure cache RAM 514 is provided in each of the components 303A-D, the information stored in the RAM 514 is very different from the subject matter of the present claims. Pending claim 1 recites "causing to store information *describing a structure of [a] queue* in a cache memory implemented in a distributed manner." In contrast, the information stored in the data structure cache RAM 514 of the Westbrook et al. patent relates to the *location of packet headers* (provided by local and global data structures 440, 450). Clearly, the location of packet headers is different from information "describing a structure of a queue." Accordingly, it would not have been obvious to one of ordinary skill in the art to implement the arrangement of cache RAM 514, as disclosed by the Westbrook et al. patent, in the device of the Starr et al. patent.

In addition, the applicant notes that the arrangement of cache RAM 514 in the Westbrook et al. patent is used for reassembling data packets that are out of order. In contrast, the Starr et al. patent does not disclose or suggest that information describing a structure of a queue is out of order or needs to be reassembled. At least for this additional reason, it would not have been

obvious to combine the arrangement of cache RAM as disclosed by the Westbrook et al. patent with the queue system of the Starr et al. patent.

At least for the foregoing reasons, claim 1 should be allowed.

Claims 2-8, 29 and 30 depend from claim 1 and should be allowed for at least the same reasons.

Independent claim 9 recites an apparatus that includes a queue manager configured to process a "request to a queue while a previous request with respect to the same queue is being processed" and a cache memory distributed partially to a memory controller in which the cache memory stores "data describing a structure of [the] queue." As discussed above, neither the Westbrook et al. patent nor the Starr et al. patent discloses or suggests a queue manager configured to process a "request to a queue while a previous request with respect to the same queue is being processed." Furthermore, for the reasons discussed above in regards to claim 1, it would not have been obvious to combine the cited references to obtain the subject matter of present claim 9.

Claims 10-13 and 31 depend from claim 9 and should be allowed for at least the same reasons as claim 9.

Independent claim 15 also recites a system that includes a queue manager configured to process "a request to a queue while a previous request with respect to the same queue is being processed" and a cache memory distributed partially to a memory controller in which the cache memory stores "data describing a structure of [the] queue." Accordingly, claim 15 should be allowed for the same reasons as claim 9.

Claims 16-19 and 33 depend from claim 15 and should be allowed for at least the same reasons as claim 15.

Independent claim 21 recites a computer-readable medium that includes computer-readable instructions to "commence processing of a received enqueue or dequeue request with respect to a queue prior to completion of processing a prior enqueue or dequeue request with

respect to the same queue" and to "store information that describes a structure of the queue in a distributed cache memory."

As discussed above, neither the Starr et al. patent nor the Westbrook et al. patent discloses or suggests processing of a received enqueue or dequeue request with respect to a queue prior to completion of processing a prior enqueue or dequeue request with respect to the same queue. Furthermore, for the reasons discussed above in regards to claim 1, it would not have been obvious to combine the cited references to obtain the subject matter of present claim 21.

Claims 22-28 depend from claim 21 and should be allowed for at least the same reasons as claim 21.

Conclusion

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper.

The amount of $50 in payment of the excess claims fee is being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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